In the Claims:

1. (Currently Amended) A MOS transistor comprising:

a an inverted T-shaped gate electrode on a substrate, the gate electrode comprising a silicon base portion and a silicon column portion extending from the base portion, the base portion and the column portion doped with a same dopant material, the base portion of the gate electrode including ~~having~~ a first lateral protrusion extending laterally beyond ~~from a lower portion of~~ a first sidewall of the column portion of the gate electrode and a second lateral protrusion extending laterally beyond ~~from a lower portion of~~ a second sidewall of the column portion of the gate electrode;

a drain region in the substrate comprising a first lightly-doped drain region under the first lateral protrusion, a second lightly-doped drain region that is deeper than the first lightly-doped drain region adjacent the first lightly-doped drain region, and a heavily-doped drain region adjacent to the second lightly-doped drain region; and

a source region in the substrate comprising a first lightly-doped source region under the second lateral protrusion, a second lightly-doped source region that is deeper than the first lightly-doped source region adjacent the first lightly-doped source region, and a heavily-doped source region adjacent to the second lightly-doped source region.

2. (Original) The MOS transistor of Claim 1, further comprising an insulating gate spacer covering the first and second sidewalls of the gate electrode, wherein the second lightly-doped drain region and the second lightly-doped source region are under bottom portions of the insulating gate spacer.

3. (Original) The MOS transistor of Claim 2, wherein the heavily doped drain region is adjacent a first outer sidewall of the insulating gate spacer and wherein the heavily doped source region is adjacent a second outer sidewall of the insulating gate spacer.

4. (Currently Amended) The MOS transistor of Claim ~~1~~ 2, ~~wherein the gate electrode has an inverted T shape~~ wherein a bottom surface of the insulating gate spacer is on a curing thermal oxide layer.

5. (Currently Amended) The MOS transistor of Claim 1, further comprising a gate dielectric layer interposed between the gate electrode and the substrate, wherein a first sidewall of the gate dielectric is aligned with a sidewall of the first lateral protrusion of the gate electrode and wherein a second sidewall of the gate dielectric is aligned with a sidewall of the second lateral protrusion of the gate electrode.

6. (Currently Amended) The MOS transistor of Claim ~~2~~ 5, further comprising a curing thermal oxide layer on the sidewalls of the gate electrode, the first and second sidewalls of the gate dielectric, the second lightly-doped drain region and the second lightly-doped source region.

7. (Original) The MOS transistor of Claim 6, wherein the insulating gate spacer is on the curing thermal oxide layer.

8. (Original) The MOS transistor of Claim 7, further comprising a spacer etch stop layer interposed between the insulating gate spacer and the curing thermal oxide layer.

9. (Original) The MOS transistor of Claim 1, wherein the sidewalls of the first and second lateral protrusions are vertically profiled.

10. (Withdrawn) The MOS transistor of Claim 1, wherein the sidewalls of the first and second lateral protrusions are sloped at positive angles.

11. (Witrhdrawn) The MOS transistor of claim 1 wherein the sidewalls of the first and second lateral protrusions are sloped at negative angles.

12. (Original) The MOS transistor of claim 1 further comprising a metal silicide layer on the upper surface of the gate electrode, the surface of the heavily-doped drain region and the surface of the heavily-doped source region.

13-53. (Cancelled)

54. (New) The MOS transistor of Claim 5, wherein the depth of the second lightly-doped drain region is about the same as the combined depth of the first lightly-doped drain region, the gate dielectric layer and the base portion of the inverted T-shaped gate electrode.

55. (New) The MOS transistor of Claim 1, wherein the base portion and the column portion of the gate electrode are not selectively etchable.